



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/515,348	02/29/2000	Christopher A. Spence	F0039	2076
45305	7590	09/10/2004	EXAMINER	
RENNER, OTTO, BOISSELLE & SKLAR, LLP (AMDS)			WERNER, BRIAN P	
1621 EUCLID AVE - 19TH FLOOR			ART UNIT	
CLEVELAND, OH 44115-2191			PAPER NUMBER	

2621

DATE MAILED: 09/10/2004

15

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/515,348

Applicant(s)

SPENCE, CHRISTOPHER A.

Examiner

Brian P. Werner

Art Unit

2621

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 25 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 25, 2004 (Amendment B) has been entered. Claims 1-24 are now pending.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 21 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 21, the original disclosure lacks written description support for the "simulated wafer structure" and the "second simulated wafer structure" being from different wafer layers. The closest support for this subject matter appears to be at

Art Unit: 2621

specification page 21, line 11, which states, “[i]n one embodiment it may be desirable to overlay the images of structures formed at various stages and layers on the wafer.”

However, claim 21 requires that the “simulated wafer structure”, which is created from the mask image data in claim 1, and the “second simulated wafer structure” of claim 2 are structures corresponding to different layers of the wafer. There is no support for this in the specification. Specification page 21, line 11 does not make it clear that these “layers” are in fact “simulated” layers corresponding to the “simulated wafer structure” and “second simulated wafer structure”. In fact, the specification appears to distinguish the “layers” embodiment of line 11 from the simulated wafer structure. That is, page 21, line 9 states, “In addition to overlaying the two images discussed above (i.e., the simulated images) ...”. Thus, it would appear that the “layers” embodiment are separate from the “simulated wafer structure” and “second simulated wafer structure” embodiment. In order to overcome this statutory rejection, the applicant is invited to point to exactly where the original disclosure teaches that the “simulated wafer structure” and the “second simulated wafer structure” of claim 2 each represent different wafer layers; or to cancel the claimed subject matter.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 7-11, 13-15 and 17-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (US 6,757,645 B2).

Regarding independent claims 1, 17 and 19, Chang discloses a method of analyzing a wafer manufacturing process (figures 4 and 6(b); “inspection of defects on masks” at column 1, line 21) comprising:

imaging a portion of a mask used in the wafer structure formation process (figure 4, numeral 430; figure 6(b), numerals 604 and 655; “reference data 655 may comprise ... an image of a similar mask” at column 16, line 66 – column 17, line 2); and

simulating lithographic processing (figure 6(b), numeral 600; “image generator 600 provides an image simulation output” at column 17, line 5) using data received from or derived from the imaging of the portion of the mask (as depicted in figure 6(b)), thereby obtaining a simulated wafer structure (the output of the generator 600 is a simulation; “simulation output” at column 17, line 5); and

evaluating the portion of the mask by comparing the simulated wafer structure with a resulting wafer structure (figure 6(b), numeral 680; “difference device 680 takes the difference between the real result 650 and the output of the summing device 675” at column 17, line 43),

wherein the resulting wafer structure is an ideal layer structure on a wafer (this limitation is met in two ways: First, the image of a “mask which has been determined to be free from defects” at column 17, line 1, stored in figure 6(b) at numeral 655, is passed to a simulator 610 which simulates the actual photoresist characteristics of a defect free wafer, which in turn is used as the “real results” a numeral 650 to which the simulation at numeral 675 is compared at numeral 680; thus, the “real results” at numeral 650 is a “result” of a photoresist exposure representing an ideal situation where the mask has not defects; Second, an actual image of a defect free photoresist image at figure 6(b), numeral 636, may be used as the “real results” at numeral 650).

Regarding claim 2, the simulated wafer structure (i.e., figure 6(b), numeral 600/675) is further compared to a second simulated wafer structure (figure 6(b), numeral 640; in addition to a comparison with a photoresist result at numeral 630, an additional comparison with an etch simulation at numeral 640 is anticipated; see “may be chosen by the user” at column 17, line 15, and “take photoresist and/or etching parameters into account” at column 15, line 59; these passages of the Chang disclosure conveys to one of ordinary skilled in the art that the user may compare with the photoresist simulation first, and then the etching simulation).

Regarding claim 3, a lithographic process is simulated (figure 6(b), numeral 20).

Art Unit: 2621

Regarding claim 7, the same simulation method is used (figure 6(b), numerals 600 at the top of the figure and the bottom left of the figure both represent the same simulation engine).

Regarding claims 8, 18 and 20, aerial image simulation is disclosed (the "Hopkins model" is used at column 12, line 55, and it is an aerial simulation; i.e., see "Fast Aerial Image Computation" at column 13, line 30).

Regarding claim 9, different simulation methods are also used (i.e., figure 6(b), numeral 620 adds an etching simulation to the simulation of numeral 600).

Regarding claims 21 and 24, the first and second simulated wafer structure are from different wafer layers and different stages of wafer formation (figure 6(b), numerals 610 and 620 represent resist and etched layers which are different layers formed at different times/steps during wafer formation).

Regarding claim 22, a comparison is disclosed as discussed above (i.e., figure 6(b), numeral 680).

Regarding independent claim 1 again, this claim is met by another embodiment of Chang at figure 9. Chang discloses:

imaging a portion of a mask used in the wafer structure formation process (numeral 915); and

simulating lithographic processing using data received from or derived from the imaging of the portion of the mask, thereby obtaining a simulated wafer structure (numeral 950); and

evaluating the portion of the mask by comparing the simulated wafer structure with a resulting wafer structure (numeral 980),

wherein the resulting wafer structure is an ideal layer structure on a wafer (numeral 910 is passed to 955 for subsequent comparison with 950 at 980; numeral 910 represents ideal design data).

Regarding claims 10 and 23, the simulated wafer structure is displayed (“displaying the images 970 and 975” at column 21, line 13).

Regarding claim 11, overlapping images are displayed (figure 20, numeral 2030).

Regarding claims 13-15, a SEM is used to generated the image as applied to claim 1 (“scanning electron microscope” at column 10, numeral 12).

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Kamon (US 5,815,685 A).

Regarding independent claim 1, Kamon discloses a method of analyzing a wafer manufacturing process (figure 4; “light proximity effect correction ... during production processes of an integrated circuit” at column 1, line 55) comprising:

imaging a portion of a mask used in the wafer structure formation process (figure 4, numeral 10; “optical image measurement unit 10 ... measuring the image projected onto a wafer via a mask produced according to the design data” at column 5, lines 58-63); and

simulating lithographic processing using data received from or derived from the imaging of the portion of the mask, thereby obtaining a simulated wafer structure (figure



Art Unit: 2621

4, numeral 4; “prediction unit 4 for predicting the pattern which will be formed in a resist as a result of the pattern transfer process” at column 4, line 62); and

evaluating the portion of the mask by comparing the simulated wafer structure with a resulting wafer structure (figure 4, numeral 5),

wherein the resulting wafer structure is an ideal layer structure on a wafer (at figure 4, numeral 5, the simulated wafer structure from numeral 4 is compared at numeral 5 with the design data from numeral 1 which represents the ideal wafer structure).

7. Claims 1-3, 7-9, 13-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Pierrat et al. (US 6,091,845 A) and Kamon (US 5,815,685 A).

Regarding claim 1, Pierrat discloses a method of analyzing a wafer manufacturing process (“semiconductor devices ... detecting defects introduced during the photolithography process” at column 1, lines 5-7; “wafers” at column 1, line 18) comprising:

imaging a portion of a mask used in the wafer structure formation process (figure 1, numeral 130 and figure 3, numeral 230); and

simulating lithographic processing (figure 1, numeral 180 and figure 3, numerals 240, 250 and 260) using data received from or derived from the imaging of the portion of the mask (as seen in figures 1 and 3, the simulation directly uses the image of the mask), thereby obtaining a simulated wafer structure (e.g., “simulated image” at column

5, line 22 comprises simulated structure, such as “elevation data” at column 5, line 56 and “sidewalls” at column 6, line 5); and

evaluating the portion of the mask by comparing the simulated wafer structure with a resulting wafer structure (figure 3, numeral 270; the simulated wafer structure at numeral 260 is compared with the “result” of a simulation using design data at numeral 365, where the design data represents the desired wafer structure),

wherein the resulting wafer structure is an ideal layer structure on a wafer (the “resulting” wafer structure at numeral 265 represents the ideal case where the mask has no negative effect on the pattern transfer; for example, looking at figure 5, the original design data 310 is simulated at 315 and is depicted at 320; then a mask is created, from which an image is picked up and simulated at 345; it can be seen that the ideal case at 320 differs from the actual mask image simulation at 350, where a defect is introduced by the mask at 332; the comparison reveals this at 360; thus, the “resulting” wafer structure at numeral 265 indeed represents the ideal layer structure on the wafer).

Regarding claim 2, the method comprises comparing (figure 3, numeral 270) the simulated structure (i.e., figure 3, numeral 260) to a second simulated structure (figure 3, numeral 265).

Regarding claim 3, the second simulated structure uses mask design data (figure 3, numeral 210).

Regarding claim 7, a same simulation method is used (figure 3, the same convolution and resist simulations are used; i.e., refer to numerals 250, 255, 260 and

265; Additionally, a separate embodiment is disclosed at figure 4, where the exact same simulations are performed in parallel, as depicted by numerals 230-262).

Regarding claim 8, the first and second simulations are aerial simulations (the Pierrat simulations are aerial simulations; e.g., an "aerial image measurement system" at column 5, line 8 is used to capture the mask image from which the aerial simulation is performed; the "simulation program logic is written in the C programming language" at column 6, line 16).

Regarding claim 9, a simulation step is applied to the imaged data (i.e., figure 3, numeral 240), where this step is not applied to the mask data (as depicted in figure 3). Thus, the overall simulation processes of the mask data and the imaged data are different.

Regarding claim 13, a SEM is used to capture the mask image ("SEM" at column 5, line 6).

Regarding claim 14, the SEM data is transformed into computer readable data (i.e., an electron image is transformed into the computer readable format required by the simulator; stated another way, a computer cannot manipulate an electron image direction, thus there must be some transformation of the electron image into a format required by the simulator).

Regarding claims 15 and 16, image analysis ("analyzes" at column 6, line 6) and scaling ("pixel erosion" at column 8, line 67; such an erosion algorithm reduces the size of a feature by eroding it away) of the data are performed.

Regarding claim 17, optical data is transformed into numerical computer data as depicted in figure 1 (i.e., light from 110 is passed through mask 161 and converted by sensor 130 to computer readable data).

Regarding dependent claim 18, an aerial image simulation program is disclosed (the Pierrat simulation is an aerial simulation; e.g., an "aerial image measurement system" at column 5, line 8 is used to capture the mask image from which the aerial simulation is performed; the "simulation program logic is written in the C programming language" at column 6, line 16).

Regarding dependent claim 19, the simulating includes simulating the developed resist image ("elevation data" at column 5, line 56 and "sidewalls" at column 6, line 5, both of which correspond to the "resist layer" at column 5, line 62, are simulated using "algorithms which emulate the behavior of resist material" at column 5, line 65).

Regarding claim 20, the simulating uses an aerial image microscope system (an "aerial image measurement system" at column 5, line 8 is used to capture the mask image from which the aerial simulation is performed; given that the structures of the mask being captured by Pierrat are extremely small, one of ordinary skill would understand that the "aerial image measurement system" is a microscope system).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1-3, 7-9, 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Pierrat et al. (US 6,091,845 A) and Kamon (US 5,815,685 A).

Regarding claim 1, Pierrat discloses a method of analyzing a wafer manufacturing process ("semiconductor devices ... detecting defects introduced during the photolithography process" at column 1, lines 5-7; "wafers" at column 1, line 18) comprising:

imaging a portion of a mask used in the wafer structure formation process (figure 1, numeral 130 and figure 3, numeral 230); and

simulating lithographic processing (figure 1, numeral 180 and figure 3, numerals 240, 250 and 260) using data received from or derived from the imaging of the portion of the mask (as seen in figures 1 and 3, the simulation directly uses the image of the mask), thereby obtaining a simulated wafer structure (e.g., "simulated image" at column 5, line 22 comprises simulated structure, such as "elevation data" at column 5, line 56 and "sidewalls" at column 6, line 5).

Even if Pierrat did not teach evaluating the portion of the mask by comparing the simulated wafer structure with a resulting wafer structure, wherein the resulting wafer structure is an ideal layer structure on a wafer, this is taught by Kamon as described in the 102(b) rejection above.

That is, Kamon discloses a system in the same field of endeavor of analyzing a wafer manufacturing process (figure 4; "light proximity effect correction ... during production processes of an integrated circuit" at column 1, line 55) comprising:

evaluating the portion of the mask by comparing (figure 4, numeral 5) a simulated wafer structure (figure 4, numeral 4) with a resulting wafer structure (figure 4, numeral 1), wherein the resulting wafer structure is an ideal layer structure on a wafer (at figure 4, numeral 5, the simulated wafer structure from numeral 4 is compared at numeral 5 with the design data from numeral 1 which represents the ideal wafer structure).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Pierrat, by comparing Pierrat's simulated wafer structure (e.g., figure 1, numeral 180) with an ideal layer structure as taught by Kamon, in order to alleviate "the deformation of patterns due to light proximity effects during production" (Kamon, column 1, line 55) thereby feeding back information to produce a photomask that achieves a more accurate wafer image.

Regarding claim 2, the method comprises comparing (figure 3, numeral 270) the simulated structure (i.e., figure 3, numeral 260) to a second simulated structure (figure 3, numeral 265).

Regarding claim 3, the second simulated structure uses mask design data (figure 3, numeral 210).

Regarding claim 7, a same simulation method is used (figure 3, the same convolution and resist simulations are used; i.e., refer to numerals 250, 255, 260 and 265; Additionally, a separate embodiment is disclosed at figure 4, where the exact same simulations are performed in parallel, as depicted by numerals 230-262).

Regarding claim 8, the first and second simulations are aerial simulations (the Pierrat simulations are aerial simulations; e.g., an "aerial image measurement system" at column 5, line 8 is used to capture the mask image from which the aerial simulation is performed; the "simulation program logic is written in the C programming language" at column 6, line 16).

Regarding claim 9, a simulation step is applied to the imaged data (i.e., figure 3, numeral 240), where this step is not applied to the mask data (as depicted in figure 3). Thus, the overall simulation processes of the mask data and the imaged data are different.

Regarding claim 13, a SEM is used to capture the mask image ("SEM" at column 5, line 6).

Regarding claim 14, the SEM data is transformed into computer readable data (i.e., an electron image is transformed into the computer readable format required by the simulator; stated another way, a computer cannot manipulate an electron image direction, thus there must be some transformation of the electron image into a format required by the simulator).

Regarding claims 15 and 16, image analysis ("analyzes" at column 6, line 6) and scaling ("pixel erosion" at column 8, line 67; such an erosion algorithm reduces the size of a feature by eroding it away) of the data are performed.

Regarding claim 17, optical data is transformed into numerical computer data as depicted in figure 1 (i.e., light from 110 is passed through mask 161 and converted by sensor 130 to computer readable data).

Regarding dependent claim 18, an aerial image simulation program is disclosed (the Pierrat simulation is an aerial simulation; e.g., an "aerial image measurement system" at column 5, line 8 is used to capture the mask image from which the aerial simulation is performed; the "simulation program logic is written in the C programming language" at column 6, line 16).

Regarding dependent claim 19, the simulating includes simulating the developed resist image ("elevation data" at column 5, line 56 and "sidewalls" at column 6, line 5, both of which correspond to the "resist layer" at column 5, line 62, are simulated using "algorithms which emulate the behavior of resist material" at column 5, line 65).

Regarding claim 20, the simulating uses an aerial image microscope system (an "aerial image measurement system" at column 5, line 8 is used to capture the mask image from which the aerial simulation is performed; given that the structures of the mask being captured by Pierrat are extremely small, one of ordinary skill would understand that the "aerial image measurement system" is a microscope system).



Art Unit: 2621

10. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Pierrat et al. (US 6,091,845 A) and Sheng (US 6,477,265 A).

Pierrat discloses generating first and second simulated structures as described above, whereby the structures are aligned and compared for defects (figure 1, numeral 140 and figure 3, numeral 270).

Regarding claims 10 and 11, Pierrat does not disclose displaying the first and second simulated structures on a display screen, at least partially overlapping one another.

Sheng discloses a photolithographic inspection system (Abstract, line 2), comprising the comparison of two image images to detect differences that are defects (figure 5; "defect detection" at column 3, line 56), wherein Sheng teaches displaying the first and second images on a display screen, at least partially overlapping one another ("image display 44 displays the superimposed image" at column 3, line 41).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to superimpose and display the first and second simulated images of Pierrat, as taught by Sheng, so that in fulfilling Pierrat's requirement for defect inspection, the images of Pierrat "can easily be inspected for defects" (Sheng, column 2, line 21, line 25, and column 3, line 61).

11. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Pierrat et al. (US 6,091,845 A) and Sheng (US 6,477,265 A) as applied to claim 11 above, and further in combination with Fiekowsky (US 6,263,292 B1).

The Pierrat and Sheng combination as applied to claim 11 discloses comparing images of two simulated structures for differences due to defects.

The Pierrat and Sheng combination does not disclose providing a user with an option of selecting a figure of merit by which critical dimension variations between the simulated structures are to be calculated.

Fiekowsky discloses a mask inspection system (figure 1; "mask" at column 10, line 58), comprising providing a user with an option of selecting a figure of merit by which critical dimension variations between the images are to be calculated ("identifying and measuring a variety of features such as defects and line widths" at column 11, line 30; "user region of interest" at column 11, line 42; "the operator is able to enter review mode and to quickly surround spot 71 with a rough user region of interest 72 indicating the region that the user wishes to analyze and measure" at column 11, lines 47-50).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Pierrat and Sheng combination as applied to claim 11, by providing a user selected figure of merit (e.g., "line widths ... heights" at column 4, Fiekowsky lines 21-22; "diameters" at Fiekowsky column 3, line 64) as taught by Fiekowsky, in order to provide "a measurement tool that provides an objective, practical and fast method for accurate sizing of mask features found with an automatic inspection tool" (Fiekowsky, column 3, lines 61-64).

12. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Pierrat et al. (US 6,091,845 A) and Fiekowsky (US 6,263,292 B1).

Art Unit: 2621

Pierrat, as applied to claims 1-3 above, discloses comparing images of two simulated structures for differences due to defects.

Regarding claim 4, Pierrat does not disclose providing a user with an option of selecting a figure of merit by which critical dimension variations between the simulated structures are to be calculated.

Regarding claim 5, line width is not disclosed.

Regarding claim 6, percentage of a difference in area is not disclosed.

Regarding claims 4 and 5, Fiekowsky discloses a mask inspection system (figure 1; "mask" at column 10, line 58), comprising providing a user with an option of selecting a figure of merit by which critical dimension variations between the images are to be calculated ("identifying and measuring a variety of features such as defects and line widths" at column 11, line 30; "user region of interest" at column 11, line 42; "the operator is able to enter review mode and to quickly surround spot 71 with a rough user region of interest 72 indicating the region that the user wishes to analyze and measure" at column 11, lines 47-50).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Pierrat, by providing a user selected figure of merit (e.g., "line widths ... heights" at column 4, Fiekowsky lines 21-22; "diameters" at Fiekowsky column 3, line 64) as taught by Fiekowsky, in order to provide "a measurement tool that provides an objective, practical and fast method for accurate sizing of mask features found with an automatic inspection tool" (Fiekowsky, column 3, lines 61-64).

Regarding claim 6, percentage of a difference area is one of many measures of differences between features that is well known, and would have been obvious to one of ordinary skill in the art in order to determine the extent of the difference.

13. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Pierrat et al. (US 6,091,845 A) and Kamon (US 5,815,685 A), and further in combination with Sheng (US 6,477,265 A).

The Pierrat and Kamon combination discloses generating first and second simulated structures as described above, whereby the structures are aligned and compared for defects (figure 1, numeral 140 and figure 3, numeral 270).

Regarding claims 10 and 11, Pierrat does not disclose displaying the first and second simulated structures on a display screen, at least partially overlapping one another.

Sheng discloses a photolithographic inspection system (Abstract, line 2), comprising the comparison of two image images to detect differences that are defects (figure 5; "defect detection" at column 3, line 56), wherein Sheng teaches displaying the first and second images on a display screen, at least partially overlapping one another ("image display 44 displays the superimposed image" at column 3, line 41).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to superimpose and display the first and second simulated images of the Pierrat and Kamon combination, as taught by Sheng, so that in fulfilling Pierrat's

Art Unit: 2621

requirement for defect inspection, the images of Pierrat "can easily be inspected for defects" (Sheng, column 2, line 21, line 25, and column 3, line 61).

14. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Pierrat et al. (US 6,091,845 A), Kamon (US 5,815,685 A) and Sheng (US 6,477,265 A) as applied to claim 11 above, and further in combination with Fiekowsky (US 6,263,292 B1).

The Pierrat, Kamon and Sheng combination as applied to claim 11 discloses comparing images of two simulated structures for differences due to defects.

The Pierrat, Kamon and Sheng combination does not disclose providing a user with an option of selecting a figure of merit by which critical dimension variations between the simulated structures are to be calculated.

Fiekowsky discloses a mask inspection system (figure 1; "mask" at column 10, line 58), comprising providing a user with an option of selecting a figure of merit by which critical dimension variations between the images are to be calculated ("identifying and measuring a variety of features such as defects and line widths" at column 11, line 30; "user region of interest" at column 11, line 42; "the operator is able to enter review mode and to quickly surround spot 71 with a rough user region of interest 72 indicating the region that the user wishes to analyze and measure" at column 11, lines 47-50).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Pierrat, Kamon and Sheng combination as applied to claim 11, by providing a user selected figure of merit (e.g., "line widths ... heights" at column

4, Fiekowsky lines 21-22; "diameters" at Fiekowsky column 3, line 64) as taught by Fiekowsky, in order to provide "a measurement tool that provides an objective, practical and fast method for accurate sizing of mask features found with an automatic inspection tool" (Fiekowsky, column 3, lines 61-64).

15. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Pierrat et al. (US 6,091,845 A) and Kamon (US 5,815,685 A), and further in combination with Fiekowsky (US 6,263,292 B1).

Pierrat, as applied to claims 1-3 above, discloses comparing images of two simulated structures for differences due to defects.

Regarding claim 4, the Pierrat and Kamon combination does not disclose providing a user with an option of selecting a figure of merit by which critical dimension variations between the simulated structures are to be calculated.

Regarding claim 5, line width is not disclosed.

Regarding claim 6, percentage of a difference in area is not disclosed.

Regarding claims 4 and 5, Fiekowsky discloses a mask inspection system (figure 1; "mask" at column 10, line 58), comprising providing a user with an option of selecting a figure of merit by which critical dimension variations between the images are to be calculated ("identifying and measuring a variety of features such as defects and line widths" at column 11, line 30; "user region of interest" at column 11, line 42; "the operator is able to enter review mode and to quickly surround spot 71 with a rough user

region of interest 72 indicating the region that the user wishes to analyze and measure” at column 11, lines 47-50).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Pierrat and Kamon combination, by providing a user selected figure of merit (e.g., “line widths ... heights” at column 4, Fiekowsky lines 21-22; “diameters” at Fiekowsky column 3, line 64) as taught by Fiekowsky, in order to provide “a measurement tool that provides an objective, practical and fast method for accurate sizing of mask features found with an automatic inspection tool” (Fiekowsky, column 3, lines 61-64).

Regarding claim 6, percentage of a difference area is one of many measures of differences between features that is well known, and would have been obvious to one of ordinary skill in the art in order to determine the extent of the difference.

### ***Response to Arguments***

16. Each of the remarks and/or arguments filed with the aforementioned amendment have been considered:

#### **Summary of Applicant's Remarks (Response Page 6)**

“Pierrat also discloses a did-to-die inspection system.” “However, Pierrat does not disclose evaluating a photomask by comparing a simulated wafer structure to a resulting wafer structure, wherein the resulting wafer structure is an ideal target layer structure on a wafer.”

Examiner's Response

First, Pierrat meets this requirement as follows:

evaluating the portion of the mask by comparing the simulated wafer structure with a resulting wafer structure (figure 3, numeral 270; the simulated wafer structure at numeral 260 is compared with the "result" of a simulation using design data at numeral 365, where the design data represents the desired wafer structure),

wherein the resulting wafer structure is an ideal layer structure on a wafer (the "resulting" wafer structure at numeral 265 represents the ideal case where the mask has no negative effect on the pattern transfer; for example, looking at figure 5, the original design data 310 is simulated at 315 and is depicted at 320; then a mask is created, from which an image is picked up and simulated at 345; it can be seen that the ideal case at 320 differs from the actual mask image simulation at 350, where a defect is introduced by the mask at 332; the comparison reveals this at 360; thus, the "resulting" wafer structure at numeral 265 indeed represents the ideal layer structure on the wafer).

Second, while claim 1 does not define the "resulting" wafer structure as a simulation, it is clear from the disclosure and from dependent claim 2 and 3 that it is. That is, specification page 11, line 24 states, "the simulator 115 may also be able to create simulated wafer structure using design data as an input, for example essentially simulation wafer fabrication with an ideal mask pattern." This is exactly what Pierrat does, for example at figure 3, numerals 255 and 265. Thus, even interpreted strictly in accord with the disclosure, Pierrat meets the requirements of a "resulting" wafer structure that is an "ideal case". Further, dependent claims 2 and 3 appear to further



limit the "resulting" wafer structure to that of a simulated wafer structure "using mask design data" (i.e., claim 3).

In summary, the Pierrat disclosure teaches the comparison of a mask image simulation with a design data simulation, and claims 2 and 3 further limit the "resulting" wafer structure to that of a simulation. This is how the claims were interpreted in the previous Office Action, and the applicant did not argue to the contrary. Thus, Pierrat meets the claimed requirements. Pierrat's comparison of simulations as depicted in figure 3 fully meet the claimed requirements.

However, a new grounds of rejection based on the Pierrat and Kamon combination is also advanced herein to address the applicant's arguments.

The arguments advanced at response page 7 and pertaining to the Garza and Pierrat combination are moot, in that the grounds of rejection is withdrawn.

The remaining arguments depend upon the claim 1 arguments, which have already been addressed above.

### ***Conclusion***

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Werner whose telephone number is 703-306-3037. The examiner can normally be reached on M-F, 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo H. Boudreau can be reached on 703-305-4706. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Werner  
Primary Examiner  
Art Unit 2621  
September 7, 2004

A handwritten signature in black ink, consisting of a series of loops and a long horizontal stroke extending to the right.

**BRIAN WERNER**  
**PRIMARY EXAMINER**